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Few-Layer Black Phosphorus Field-Effect Transistors with Reduced Current Fluctuation

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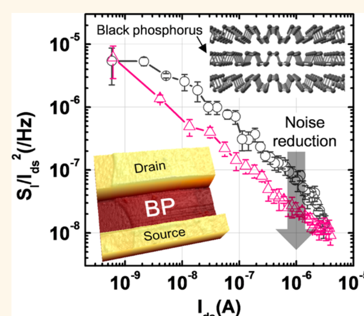
ABSTRACT We investigated the reduction of current fluctuations in few-layer black phosphorus (BP) field-effect transistors resulting from Al_2O_3 passivation. In order to verify the effect of Al_2O_3 passivation on device characteristics, measurements and analyses were conducted on thermally annealed devices before and after the passivation. More specifically, static and low-frequency noise analyses were used in monitoring the charge transport characteristics in the devices. The carrier number fluctuation (CNF) model, which is related to the charge trapping/detrapping process near the interface between the channel and gate dielectric, was employed to describe the current fluctuation phenomena. Noise reduction due to the Al_2O_3 passivation was expressed in terms of the reduced interface trap density values D_{it} and N_{it}, extracted from the subthreshold slope (SS) and the CNF model, respectively. The deviations between the interface trap density values extracted using the SS value and CNF model are elucidated in terms of the role of the Schottky barrier between the few-layer BP and metal contact. Furthermore, the preservation of the Al_2O_3-passivated few-layer BP flakes in ambient air for two months was confirmed by identical Raman spectra.



KEYWORDS: phosphorene · black phosphorus · low-frequency noise · Al_2O_3 · passivation

Tremendous interest in two-dimensional van der Waals (vdW) layered materials such as graphene,[1−3] MoS_2,[4−6] WSe_2,[7−9] and other transition-metal dichalcogenides (TMDs)[10−13] has been devoted to the field of electronic and opto-electronic applications. Because graphene suffers from the lack of a band gap, it exhibits a semimetallic property; thus, it is not suitable as a channel material in transistor and logic applications.[14,15] In 2011, monolayer MoS_2 field-effect transistors (FETs) were recorded to exhibit a high carrier mobility of ∼217 $cm^2\ V^{-1}\ s^{-1}$ and high on/off current ratio of $\sim 10^8$ owing to the suppression of Coulomb scattering in a high-*k* environment and the existence of a reasonable band gap (∼1.8 eV for monolayer and ∼1.2 eV for multilayer MoS_2), respectively.[6] This carrier mobility value was corrected later to ∼15 $cm^2\ V^{-1}\ s^{-1}$ by properly calculating the gate capacitance in a dual-gate configuration.[16,17] However, the mechanism of the high-*k* effect on vdW layered materials remains unclear; thus, relevant studies have to be continuously conducted.

Studies to enhance the carrier mobility values of MoS_2 transistors in terms of intrinsic or extrinsic treatment effects on MoS_2 are ongoing.[4] The literature on intrinsic treatments that alter the structural defects of MoS_2 such as point defects, dislocations, and so on is currently very few. Some research activities regarding the plasma treatment effects on MoS_2 were reported.[18,19] Further intensive works to obtain high-quality MoS_2 and other vdW layered materials have to be conducted. In contrast to the efforts in enhancing the intrinsic effects, extrinsic treatment approaches that improved the interface qualities between the MoS_2 and the metal electrodes or gate dielectrics are thoroughly studied. Alternative metals that form an interface with MoS_2 and are used as electrodes for devices were considered to decrease the effective Schottky barrier height and reduce the contact resistance, which is explained in terms of the work function variation and Fermi level energy pinning.[5,20,21] For example, scandium metal-contacted MoS_2 transistors recorded high

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carrier mobility values of ~184 $cm^2 V^{-1} s^{-1}$.[5] Using external dopants such as potassium,[22] polyethylenimine (PEI),[23] and benzyl viologen (BV),[24] we can also realize an increase in the MoS_2 device performance. In addition, enhancement in the interface quality between MoS_2 and the gate dielectric can also be regarded as one of the extrinsic treatment approaches to increase the carrier mobility in transistors; therefore, various gate dielectrics such as poly(methyl methacrylate) (PMMA),[25] Al_2O_3,[26] and boron nitride[27,28] have been applied to the MoS_2 devices. In various dielectric environments, for example, MoS_2 transistors encapsulated and passivated with PMMA[25] and Al_2O_3[5] showed high carrier mobility values such as ~470 and ~700 $cm^2 V^{-1} s^{-1}$ at room temperature, respectively. Currently, however, these superior carrier mobility values of MoS_2 devices discussed above require continuing studies, whose results would show comparable results to ensure reliability.

In the absence of critical intrinsic or extrinsic treatment approaches, black phosphorus (BP), another vdW layered material, has been demonstrated as a channel material that can achieve high-performance FETs with a carrier mobility value of ~1000 $cm^2 V^{-1} s^{-1}$ at room temperature, even in the form of few-layer BP transistors.[29] According to the results from another study that reported carrier mobility values on the order of 10^2 $cm^2 V^{-1} s^{-1}$,[30,31] BP materials can somewhat retain the bulk carrier mobility value in a few-layer form, in contrast to other TMDs. From this perspective, few-layer BPs are considered as a promising channel material for high-performance electronic device applications. To further increase the device performance and realize better device analysis on few-layer BP FETs, research on the effects of high-*k* layer on few-layer BPs must be profoundly pursued relative to other vdW layered materials.

The low-frequency noise (LFN) characterization method has been used as a tool for diagnosing carrier transport behavior and interface quality between a semiconductor and an insulator in conventional metal–oxide–semiconductor FETs (MOSFETs).[32−34] Other methods of obtaining interface quality information on the devices, namely, capacitance–voltage measurement and deep-level transient spectroscopy, are limited by the area size of the interface; hence, measurement using nanoscale devices becomes difficult.[34] Fortunately, LFN measurement can be applied regardless of the area size of the interface, which is one of the advantages of this method in nanodevice analysis. Because downscaling of the device can aggressively be performed, the increase in signal-to-noise ratio emphasizes the importance of LFN characterizations.[33] In addition, reduction in the noise level in the devices can affect the device performance; therefore noise-level reduction methods in vdW materials have to be developed and analyzed. To the best of our knowledge, our work on the LFN characteristics of few-layer BP FETs is the first report on this subject. We also propose a method to reduce the current fluctuations using an Al_2O_3-passivation layer.

RESULTS AND DISCUSSION

BP is one of the layered materials in which each layer is stacked with vdW interactions along the *z*-direction, as shown in Figure 1a.[29,35] The interlayer distance between the closest individual layers is estimated to be ~0.32 nm.[36] A few-layer BP can also be exfoliated from bulk BP and placed onto a Si/SiO_2 substrate, which consists of a highly p^{++} Si and a thermally oxidized 300 nm thick SiO_2 layer in this study. Representative Raman spectra (532 nm, Nd:Yag laser) of a few-layer BP onto the Si/SiO_2 substrate are shown in Figure 1b, and the Raman peak locations (A_g^1 ~361 cm^{-1}, B_{2g} ~439 cm^{-1}, and A_g^2 ~467 cm^{-1}) indicate that the material is a BP.[30,31,35] To characterize the electrical properties of few-layer BPs, an Au-only metal (~100 nm thick) was used as a source and drain electrode using subsequent electron beam lithography and thermal evaporation. The optical image of the as-fabricated few-layer BP device is shown in Figure 1c (left image). To determine the thickness of the few-layer BP, atomic force microscopy (AFM) was used, and the three-dimensional image is shown in Figure 1c (center image). The thickness of the few-layer BP was confirmed to be ~7.5 nm, as shown in Figure 1c (right image). Thermal annealing and Al_2O_3 deposition were sequentially applied to the devices, and static and LFN measurements were performed between process intervals.

Figure 2a shows the typical output characteristics of a few-layer BP FET, which is identical to that shown in Figure 1c; this device has just been thermally annealed. The ohmic-like behavior at a high gate voltage such as V_{gs} = −40 and −80 V implies that the Schottky-barrier-induced series resistances can be ignored. The trend of the gate-voltage-dependent drain current result shown in the inset of Figure 2a is opposite of the data shown in Figure 2a. This behavior matches the transfer characteristics of the few-layer BP FET shown in Figure 2b. In the region of high positive gate voltages (V_{gs} > 20 V), the electron is the dominant charge carrier; thus, the drain current increases as the gate voltage positively increases. In the region of moderate negative gate voltages (V_{gs} < 20 V), the hole becomes the dominant charge carrier; thus, the device displays p-type behavior. Similar to that shown by the graph in Figure 2b, p-branch-enhanced ambipolar characteristics appear in most of the thermally annealed few-layer BP FETs. We note that the devices used in this study are thermally annealed unless otherwise specified. Additionally, field-effect mobility (μ_{FE}) values in this study are calculated from transfer characteristics such as in Figure 2b by using $\mu_{FE} = L/(WC_{ox}V_{ds})g_m$, where W and

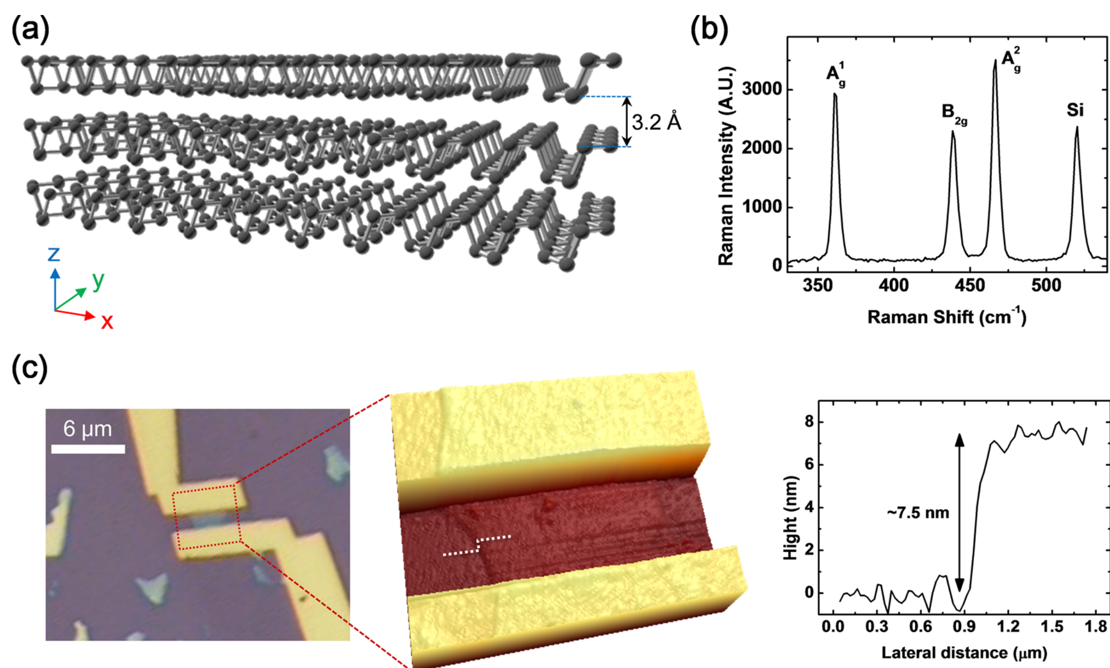

Figure 1. (a) Schematic image of a few-layer BP. (b) Raman spectrum of a few-layer BP placed on a SiO_2/Si substrate measured at room temperature and ambient air. (c) (Left) Optical image of a source/drain metal-contacted few-layer BP. (Center) Three-dimensional image of a few-layer BP with Au contact metals measured by AFM. (Right) Thickness of the few-layer BP was measured to be ∼7.5 nm.

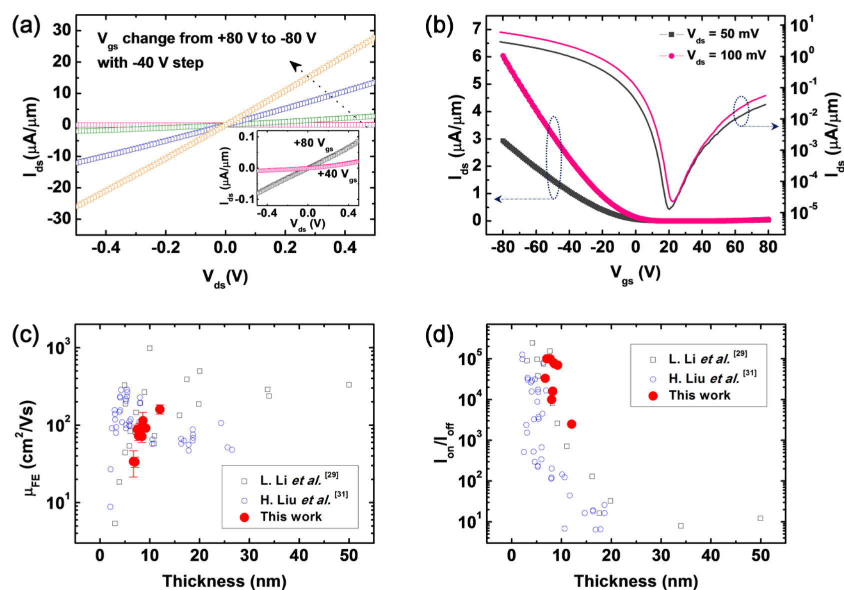

Figure 2. (a) Output characteristics of the few-layer BP FET as a function of the gate voltage. This device is the same as that shown in Figure 1c. The inset shows the same output characteristics but exhibits only those of gate voltages +80 and +40 V. The channel length and width of this device are ∼1.1 and ∼2.6 μm, respectively. (b) Corresponding transfer characteristics of the few-layer BP FET at V_{ds} = 50 mV and V_{ds} = 100 mV. (c) Field-effect mobility μ_{FE} and (d) on/off current ratio I_{on}/I_{off} data set of this study as a function of the thickness of a few-layer BP together with the digitized data from other literature.[29,31] The error bars in the μ_{FE} values are associated with various drain voltages and double-swept data in the transfer characteristics.

L are the length and width of the channel, respectively; C_{ox} is the gate capacitance per unit area; and g_m is the transconductance.

The thickness-dependent μ_{FE} and on/off current ratio of our few-layer BP FETs are shown in Figures 2c and d, respectively, along with the earlier reported data by Li *et al.*[29] and Liu *et al.*[31] The obtained results match well with the trend of the reported data. As the thickness increases within the range in our results, μ_{FE} also increases because the charge impurity scattering at the interface can be more effectively reduced in thicker samples due to the screening effect resulting from the accumulated charge carrier layer in the few-layer BP channel.[29,37] In contrast, the on/off current

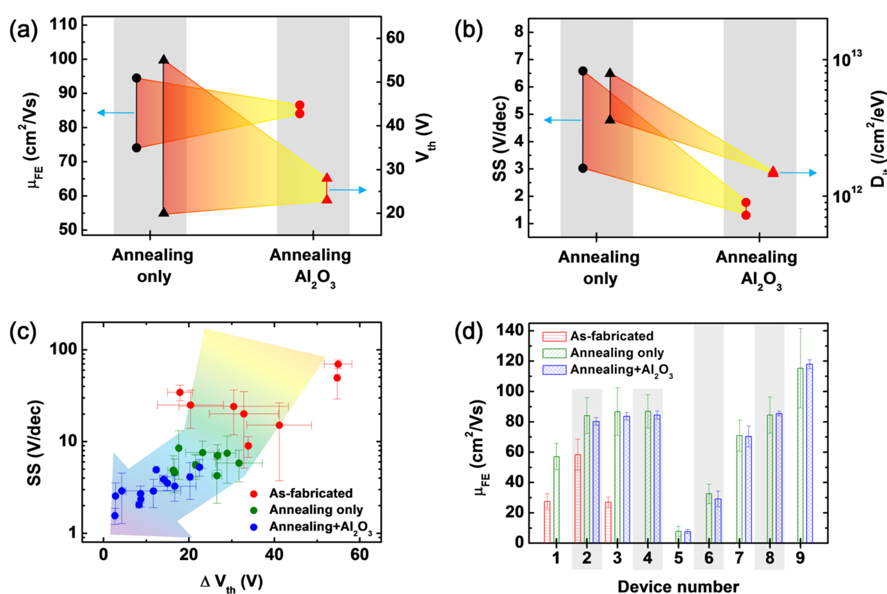

Figure 3. Static analysis and quantitative data of the few-layer BP FETs in relation to the thermal annealing and Al_2O_3-passivation effect. (a and b) μ_{FE}, V_{th}, SS, and D_{it} changes of the few-layer BP FET before and after Al_2O_3 passivation, denoted by "Annealing only" and "Annealing Al_2O_3". This device is the same as that shown in Figure 2a and b. The two different values in each case result from the double gate voltage swept data. (c) Quantitative SS and ΔV_{th} data for three cases of few-layer BP FETs: "As-fabricated", "Annealing only", and "Annealing + Al_2O_3". The ΔV_{th} values are the V_{th} difference between the double gate voltage swept data. The gradated arrow is provided for visual guidance. (d) μ_{FE} changes in three steps for each few-layer BP FET.

ratio decreases when the thickness increases, as shown in Figure 2d, which probably results from the increase in the number of independent layers in the gate voltage; that is, the charge carriers in these layers cannot be depleted using the back gate voltage.[29] When the thickness increases, the increase in the interlayer resistance reduces μ_{FE}, as described in studies related to MoS_2, due to the top-contacted geometry of the devices.[37,38] However, the interlayer resistance value of the BP is likely to be relatively smaller than that of MoS_2. Therefore, significant reduction in μ_{FE} is not observed,[29,37] which can also be considered as an advantage in terms of device operation. For logic device applications, therefore, the rational thickness of the BP layer can be ~8 nm, together with high μ_{FE} and on/off current ratio.

The μ_{FE} values shown in Figure 2c are an order of magnitude lower than the bulk mobility values for the hole ~1000 $cm^2\ V^{-1}\ s^{-1}$ at room temperature,[35] which could be attributed to several factors. First, the series resistance portion, which can be induced by the BP−metal contact interface and interlayer resistance, is one of the causes for the decrease in the extrinsic mobility.[5,37,38] Remnant molecules on the BP surface, such as oxygen and water, can be applied to the charge traps and/or scattering centers.[39,40] The imperfect interface between the BP and SiO_2 may also reduce carrier mobility.[28,41] Anisotropic conductivity in the *x* and *y* directions (in-plane; see Figure 1a) can be an obstacle in achieving the highest mobility if the electrodes are randomly fabricated regardless of the crystal direction.[35,42] In addition, structural defects and surface oxidation in the BP layer can act as scattering sites and reduce carrier mobility.[42] Recently, according to the calculation of Qiao *et al.*,[36] the phonon-limited hole mobility of a few-layer BP device with five layers can reach ~5000 $cm^2\ V^{-1}\ s^{-1}$ at room temperature. Few-layer BP devices can be more attractively applied as channel materials for FETs than any other vdW layered materials once the above-mentioned causes for the decrease in the mobility of few-layer BPs are solved using controlled methods such as appropriate high-*k* gate dielectric environment, passivation, metal electrodes, and so on.

To determine the Al_2O_3-passivation effect on few-layer BP FETs, additional static device parameters such as μ_{FE}, hysteresis, subthreshold slope (SS), and interface trap density (D_{it}) must be known. These quantitative data should also be extracted before and after the Al_2O_3 deposition, which are denoted as "Annealing only" and "Annealing Al_2O_3," respectively, in Figure 3. We note that hysteresis is defined as the threshold voltage difference (ΔV_{th}) between the transfer curves swept toward the positive and negative directions, as shown in the right axis in Figure 3a. The typical hysteretic behavior in each step in the transfer characteristics of the few-layer BP FETs is shown in Figure S1 (Supporting Information). In addition, D_{it} is normally extracted from the SS using the following relationship:[43]

$$SS = \frac{k_B T}{q} \ln 10 \left(\frac{C_{ox} + C_s + C_{it}}{C_{ox}} \right) \quad (1)$$

where q is the electronic charge; k_B is the Boltzmann constant; T is the temperature in kelvin; and C_{ox}, C_s, and

C_{it} are the gate, semiconductor, and interface-trap capacitances, respectively. C_{it} is equal to qD_{it}. The C_s can also be negligible due to the relatively thin BP layer.

The large variation among the μ_{FE} values for the annealed-only case compared with that for the Al_2O_3-passivated case is attributed to the difference between the hysteresis values in each case, as shown in Figure 3a.[42] Obviously, hysteresis also causes variations in the other device parameters such as SS and D_{it}, as shown in Figure 3b. After the Al_2O_3 passivation, the hysteresis is remarkably reduced from ~35 to ~5 V, as shown in Figure 3a, and the variations in the other parameters are accordingly reduced. Moreover, the mean values of the SS and D_{it} shown in Figure 3b are reduced from ~4.8 to ~1.5 V dec^{-1} and from ~5.7 × 10^{12} to ~1.5 × 10^{12} cm^{-2} eV^{-1}, respectively. Figure 3c shows that the quantitative changes in the SS and hysteresis values resulting from the thermal annealing and Al_2O_3-passivation effects on the device performance of the few-layer BP FETs are reliable. As-fabricated devices, *i.e.*, devices before the thermal annealing process, have high SS and hysteresis values. After the thermal annealing, the SS values are significantly reduced, but the hysteresis values are only slightly reduced. The removal of polymer residues near the BP layers[44−46] and the improvement in the contact properties[47,48] through thermal annealing can affect the reduction in the SS values. In addition, the significantly improved μ_{FE} values after thermal annealing shown in Figure 3d can also be attributed to these reasons.[44−48] Thermal annealing and electrical measurement under vacuum are not the *in situ* processes applied in this study; thus, the hysteresis values can remain if the dominant hysteresis sources are adsorbates such as water and/or oxygen molecules near the BP layers and/or the silanol groups on the SiO_2 surface.[39,49−52] Through Al_2O_3 passivation by the atomic layer deposition (ALD) process, the SS and hysteresis values are evidently reduced. The remaining water and/or oxygen molecules near the BP layers can be effectively removed during the preheating step of the ALD process (~220 °C).[49−51] Further, the sequential chemisorptions of the trimethylaluminum (TMA) precursor to the hydroxyl groups on the SiO_2 and the surface oxidation layer of the BP can also reduce the water and/or oxygen molecules and hydroxyl groups that probably affect the SS and hysteresis values.[53−55] Afterward, the 30 nm thick Al_2O_3 layer can also positively suppress the surface reactions between the BP layer and gas molecules during the device operation.[53−55] This tendency of reduced SS and hysteresis values by the Al_2O_3 deposition suggests that the Al_2O_3 passivation can be a positive method of realizing high-performance few-layer BP FETs. On one hand, the mean μ_{FE} values both before and after the Al_2O_3 passivation (Figure 3a) are almost the same. Moreover, the μ_{FE} values extracted from each step for each device remain the same after the Al_2O_3 passivation, as shown in Figure 3d. Recently, a study has reported that the fixed oxide charges in an Al_2O_3 layer can induce energy-band bending near the contact and modulate the type of operation in few-layer BP devices.[56] However, these devices had to suffer a decrease in the conductance and μ_{FE} values resulting from a large contact resistance.[56] On the other hand, the ALD Al_2O_3 layer on the few-layer BP in our study did not randomly change the type of operation of the device but improved the device performance in terms of the SS and hysteresis, whereas the μ_{FE} values remained stable, which implies that the role of the fixed oxide charges is insignificant. The unchanged μ_{FE} values after the Al_2O_3 passivation could have originated from the balanced competition of positive and negative factors: reduced adsorbates and/or hydroxyl groups during the ALD process,[53−55] suppression of Coulomb scattering due to the high-*k* screening effect,[5,6,17,26] high density of the fixed oxide charges in high-*k* dielectrics,[56,57] and remote phonon scattering of high-*k* dielectrics.[58] In fact, the effects of Al_2O_3 deposition on the devices depend on the ALD process conditions,[55,59] but we believe that this change trend in the device parameters as a result of the Al_2O_3 passivation is more reliable because the effects of the thermal annealing process are also considered.

Figure 4a shows the drain current spectral density (S_I) as a function of the frequency at different gate voltages obtained from the LFN measurement of the thermally annealed few-layer BP FET, which is the same as that shown in Figure 3a and b. These data were Fourier transformed to the frequency range on the basis of the time-domain drain current fluctuation of the device at different gate voltages, as shown in Figure 4b. The degree of drain current fluctuations appears to increase as the gate voltage negatively increases, and clear expression of the phenomena can be easily seen in Figure 4a. Correspondingly, S_I (which is normally considered as a device noise level) also increases as the gate voltage negatively increases (Figure 4a), which results in the increase in the drain current. This is a typical tendency of the LFN characteristics in devices because the more charge carriers are produced, the more charge carriers are correlated to the noise sources.

Two types of LFN models are widely accepted to well describe the noise characteristics in conventional silicon MOSFETs: carrier number fluctuation (CNF) and Hooge mobility fluctuation (HMF) models.[32,34] The CNF model suggests that current fluctuations arise from the change in the charge carrier density due to the charge trapping/detrapping phenomena at the trap sites near the channel−insulator interface. The HMF model describes that the change in the carrier mobility resulting from the variation of the scattering cross section induced current fluctuations. To figure out which type

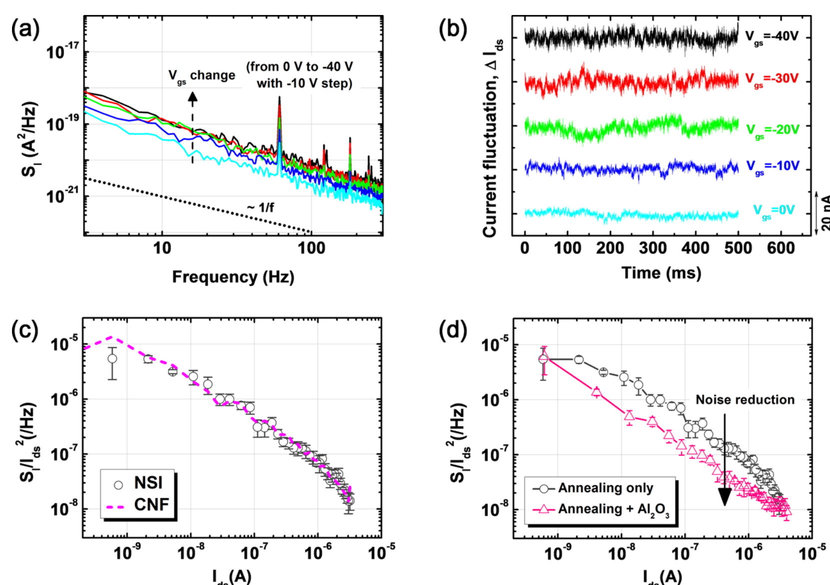

Figure 4. LFN characteristics of the few-layer BP FET, which is the same device as that shown in Figure 3a and b. (a) Drain current spectral density as a function of frequency at various gate voltages for the thermally annealed few-layer BP FET. (b) Current fluctuation in the time domain at the same gate voltage values as those in (a). (c) Mean normalized drain current spectral density (NSI) as a function of the drain current at frequencies of 8, 9, 10, 11, and 12 Hz. The corresponding CNF model is fitted to the NSI data. (d) Noise reduction due to Al_2O_3 passivation represented by the mean normalized drain spectral density as a function of the drain current before and after the Al_2O_3 passivation.

of LFN model is dominant and well expresses the carrier transport behavior in a few-layer BP FET, the normalized drain current spectral density (S_I/I_{ds}^2) as a function of the drain current is shown in Figure 4c. In the CNF model, the normalized drain current spectral density can be expressed as[32]

$$\frac{S_I}{I_{ds}^2} = \left(\frac{g_m}{I_{ds}}\right)^2 S_{Vfb} \tag{2}$$

where g_m is the gate transconductance and S_{Vfb} is the flat band voltage spectral density, which can also be expressed as

$$S_{Vfb} = \frac{q^2 k_B T N_{it}}{WLC_{ox}^2 f} \tag{3}$$

where W and L are the width and length of the channel, respectively, and N_{it} is the interface trap density. Using this CNF model, we obtain the best-fit result for the thermally annealed few-layer BP FET, as shown in Figure 4c. The thicker BP devices have lower on/off current ratio, as shown in Figure 2d; therefore, determining which type of noise model is appropriate for these devices is difficult. Different points of view may arise; however, this uncertainty is similar to the issue on why graphene FET is controversial in terms of deciding which dominant noise model is appropriate for it.[2] To further confirm the appropriate noise model for the few-layer BP device, we plot the equivalent input gate voltage spectral density (S_{Vg}) as a function of the gate voltage in Figure S2. The flat region in the accumulation regime of the FET implies that the CNF model is the appropriate noise model for the thermally annealed few-layer BP FETs because the other noise models, including the HMF and the carrier number fluctuation with correlated mobility fluctuation (CNF−CMF), are dependent on the gate voltage, presented in the Supporting Information.[32,60,61]

After the Al_2O_3 passivation on the thermally annealed few-layer BP FETs, S_I/I_{ds}, which is also considered as a noise level, is reduced over the entire device operation regime, as shown in Figure 4d. This result implies that the trap sites that activate the charge fluctuations are reduced by the Al_2O_3 passivation. According to the reduced SS and hysteresis values shown in Figure 3, we expect that the removal of the remaining adsorbates and hydroxyl group near the BP layer can affect the reduction in the noise level resulting from the suppression of the charge trapping/detrapping process. More studies regarding the specific relationship between the Al_2O_3 layer and few-layer BP FETs must be conducted; however, we should note that Al_2O_3 passivation is one way of reducing the noise level in few-layer BP FETs.

To further analyze the LFN characteristics of the Al_2O_3-passivated few-layer BP FET, the S_I/I_{ds}^2 data as a function of the drain current and the corresponding LFN models are shown in Figure S3. The CNF model does not fit in the hole accumulation regime, *i.e.*, the high positive gate voltage region. Therefore, the CNF−CMF model is introduced, which finally fits the S_I/I_{ds}^2 data all over the region, indicating that the charge trapping/detrapping process in the trap sites can change the scattering rate, resulting in the

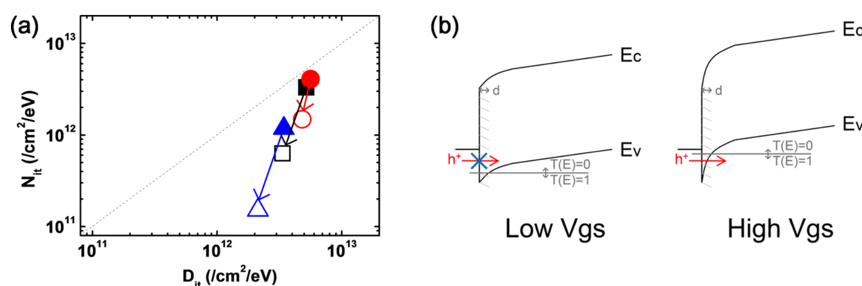

Figure 5. (a) Interface trap density values obtained from the LFN (N_{it}) and transfer (D_{it}) characteristics and changes (filled) before and (empty) after the Al_2O_3 passivation. (b) Energy band diagrams near the metal–BP contact representing the tunneling probability $T(E)$ for two regimes at low and high gate voltages.

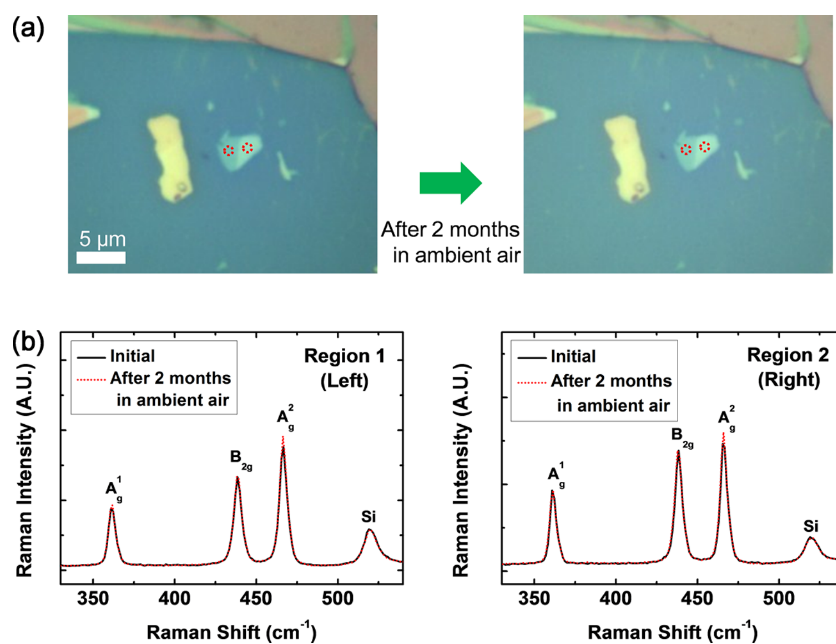

Figure 6. Al_2O_3-passivation effect on the Raman spectra of the few-layer BP. (a) Optical images of (right) the few-layer BP flakes passivated with Al_2O_3 layer and (left) the same flakes stored in ambient air after two months. (b) Raman spectra corresponding to the same few-layer BP flakes indicated by the two red and dashed circles (left and right) in (a).

fluctuation of the charge carrier mobility.[32−34] From both the CNF and CNF−CMF models, the interface trap density N_{it} can be extracted using eq 3. By dealing with the device shown in Figure 4, the N_{it} values for the thermally annealed and Al_2O_3-passivated few-layer BP FETs are obtained as $\sim$1.2 $\times$ 10^{12} and $\sim$1.5 $\times$ 10^{11} cm^{-2} eV^{-1}, respectively. These values are within the range from 10^9 to 10^{12} cm^{-2} eV^{-1} for the Si−SiO_2 and Si−high-k interface, respectively.[34]

Figure 5a shows the change in the D_{it} and N_{it} values extracted using the static and LFN analyses corresponding to eqs 1 and 3 for three different few-layer BP FETs before and after the Al_2O_3 passivation. It is noted that the D_{it} and N_{it} values were assumed to be independent of energy.[62,63] Both the D_{it} and N_{it} values are reduced after the Al_2O_3-passivation process, which is the same effect as that on the device parameters and noise level of the few-layer BP FETs discussed earlier. The D_{it} and N_{it} values are different from each other for each identical device, which can be ascribed to the following factors: first, the D_{it} value is calculated from the SS, which might be less accurate because the deep subthreshold region can be hidden in the case of an unclear off-current region. Thus, the SS values may be imprecise in this case. In the three devices in Figure 5a, however, the on/off current ratio values are over 10^4; thus, the SS deviations can be minimized. More importantly, the SS equation can be changed in Schottky barrier FETs:[64]

$$SS = \frac{k_B T}{q} \ln 10 \left(\frac{1}{2} + \frac{\lambda}{d}\right) \quad (4)$$

where λ is the screening length defined as $(\varepsilon_r \varepsilon_{ox}^{-1} t_r t_{ox})^{1/2}$ (in which ε_r and ε_{ox} are the BP and SiO_2 dielectric constants and t_r and t_{ox} are the BP and SiO_2 thicknesses, respectively) and d is the tunneling distance. The tunneling probability is zero if the width of the Schottky barrier is larger than d. Assuming that d is constant, the SS value depends on the BP and SiO_2 thicknesses, as expressed in eq 4. Thus, the SS value

cannot provide information regarding the interface trap density in this case. However, the kinked point in the transfer curve of the Schottky barrier FET, which represents the change of the carrier transport mechanism at the contact,[64,65] is not observed in our devices. Therefore, the Schottky barrier is insignificant in our devices but can still affect the SS values. It is worth noting that the SS value is extracted in the subthreshold region, which is in the low gate voltage regime; thus, the width of the Schottky barrier can be large, resulting in imprecise D_{it} values, as shown by the energy band diagrams in Figure 5b. On the other hand, the N_{it} values obtained from the LFN analysis may more precisely reflect the interface trap density information because CNF model fitting is performed on the entire device operation regime, including the high gate voltage region, as shown in Figure 4c. Therefore, analyzing the LFN characteristics of the few-layer BP FETs is needed to obtain accurate interface quality information and understand the charge carrier transport properties.

BP flakes are well known to degrade when stored in ambient air without any passivation layers.[29,30,66] This phenomenon has not been precisely investigated yet, but surface reactions with gas molecules in ambient air have been considered as a dominant factor in the degradation. To further verify the ALD Al_2O_3-passivation effect, the few-layer BP flakes passivated with an Al_2O_3 layer were stored in ambient air at room temperature for two months. The optical images and Raman spectra shown in Figure 6 confirm that the Al_2O_3 layer can effectively block the surface reactions between the BP and gas molecules in ambient air, resulting in the passivation effect on the few-layer BP flakes. This result suggests that the ALD Al_2O_3 layer can be a promising candidate in passivating few-layer BP flakes and enhancing the device performance.

CONCLUSION

In summary, current fluctuation, also considered as a noise level in devices, was reduced all over the device operation regime in few-layer BP FETs as a result of Al_2O_3 passivation. Our static analysis also confirmed the positive effects of the Al_2O_3 passivation on the devices by qualitatively and quantitatively monitoring the device parameters such as the hysteresis, SS, and D_{it}. Moreover, through a separate analysis of the thermal annealing and Al_2O_3-passivation effects, the static and LFN characteristics of few-layer BP FETs were verified to be more reliable. To analyze the LFN characteristics, we introduced the CNF model that suggests that current fluctuation is induced by the charge carrier trapping/detrapping process in the trap sites near the gate insulator. By comparing the D_{it} and N_{it} values obtained from the static and LFN analyses, respectively, we observed the same trend in which the interface trap density values decreased after the Al_2O_3 passivation. The deviation between these values was explained to be due to the Schottky barrier contact between the metal and few-layer BP flake. Finally, we confirmed through the identical Raman spectra that the Al_2O_3 passivation plays a major role in conserving the few-layer BP flakes in ambient air for two months. Our study can be applied in understanding the role of high-*k* dielectric in the performance of the few-layer BP FETs and in realizing high-performance passivated few-layer BP FETs.

EXPERIMENTAL METHODS

Thermal Annealing. First, the as-fabricated BP devices were placed onto the center of a horizontal tube furnace (Lindberg Blue from Thermo Scientific), and the chamber was depressurized to a low-vacuum level of $\sim 7 \times 10^{-2}$ Torr. This vacuum level was maintained during the entire thermal annealing process. The temperature in the chamber was sequentially increased up to 220 °C for 15 min and maintained for 5 h in the absence of any gas flows. Thereafter, the temperature was gradually decreased to room temperature.

Al_2O_3 Deposition. By applying the ALD process (Atomic Classic, CN-1 Corporation), a 30 nm thick Al_2O_3 layer was deposited on the BP devices at 220 °C for an 8 h growth duration (235 cycles at a growth rate of 1.3 Å cycle^{-1}). The aluminum and oxygen precursors were TMA (UP Chemical Co., Ltd.) and deionized water, respectively. For the carrier and purging gas, ultrapure N_2 (99.999%) was used at a rate of 200 sccm. The ALD cycle followed the sequence H_2O (1 s)/N_2 (60 s)/TMA (1 s)/N_2 (60 s). The initial vacuum level of the growth chamber was $\sim 5 \times 10^{-2}$ Torr and maintained at ~1 Torr during the deposition.

Electrical Characterization. All static and ac measurements were carried out in room temperature and high vacuum ($\sim 5 \times 10^{-5}$ Torr) using a cryogenic probe station (CPX-VF, Lakeshore). The static electrical properties of the FETs were measured using a HP 4155C semiconductor parameter analyzer. LFN measurements were performed using our custom LFN characterization system,[67] which was configured using a data acquisition module.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: The hysteretic behaviors of transfer characteristics and further LFN analyses in few-layer BP FETs are described in detail here. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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